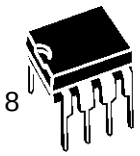
SGS-THOMSON MICROELECTRONICS

M2201

SERIAL 1K (128 x 8) EEPROM

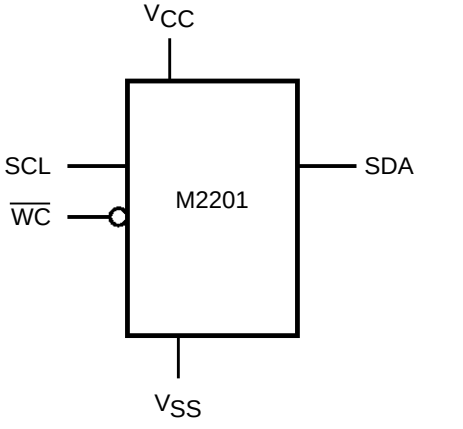
- TWO WIRE SERIAL INTERFACE
- 100.000 ERASE/WRITE CYCLES with 100 YEARS DATA RETENTION at 55°C
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for M2201 version
  - 2.7V to 5.5V for M2201W version
- HARDWARE WRITE CONTROL
- 100k BIT TRANSFER RATE
- BYTE WRITE
- PAGE WRITE (up to 4 BYTES)
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The M2201 is a simplified 2-wire bus 1K bit electrically erasable programmable memory (EEPROM), organized as 128 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees a data retention of 100 years at 55°C.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

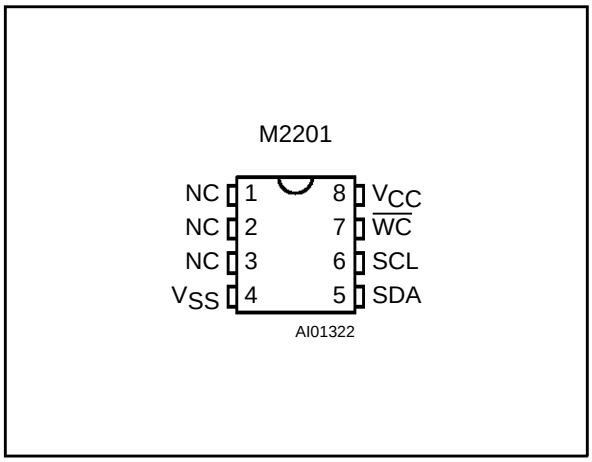
The memory is compatible with a two wire serial interface which uses a bi-directional data bus and serial clock. Read and write operations are initiated by a START condition generated by the bus master and ended by a STOP condition.

Address bits and R$\overline{W}$ bit are defined in one single byte, instead of two (or three) bytes for the standard I^2C protocol.

Table 1. Signal Names

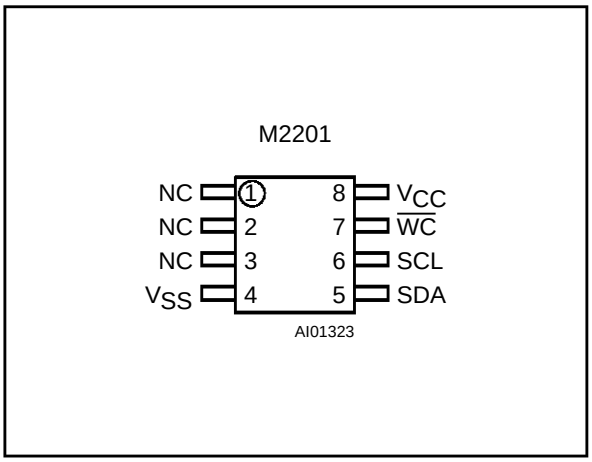
SDA	Serial Data Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = Not Connected

Figure 2B. SO Pin Connections



Warning: NC = Not Connected

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.6 to 6.5	V
V_I	Input Voltage			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

When writing data to the memory, it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} ($\overline{WC}$ is disabled).

DEVICE OPERATION

The device that controls the data transfer is known as the master. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The M2201 is always a slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the M2201 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the M2201 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the M2201 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS})

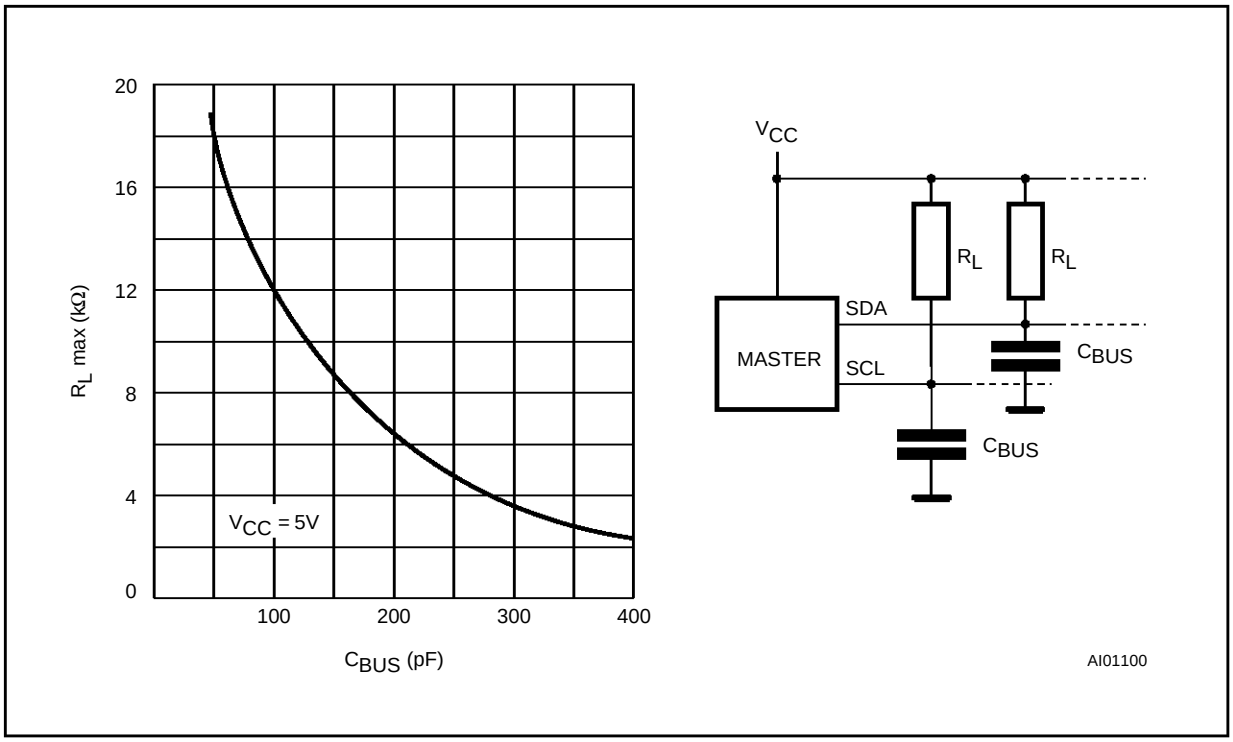


Table 3. Input Parameters (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL} (1)	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH} (1)	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP} (1)	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. The results come from simulation, actual results may vary. These figures are not guaranteed.

Table 4. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.7V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	f_C = 100kHz (Rise/Fall time < 30ns)		2	mA
I_{CC1}	Supply Current (Standby)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V

Table 5. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.7V to 5.5V)

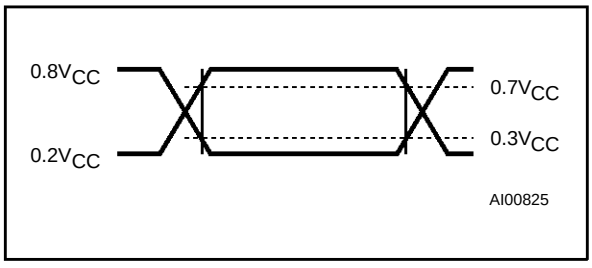
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV} (2)	t_{AA}	Clock Low to Next Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms

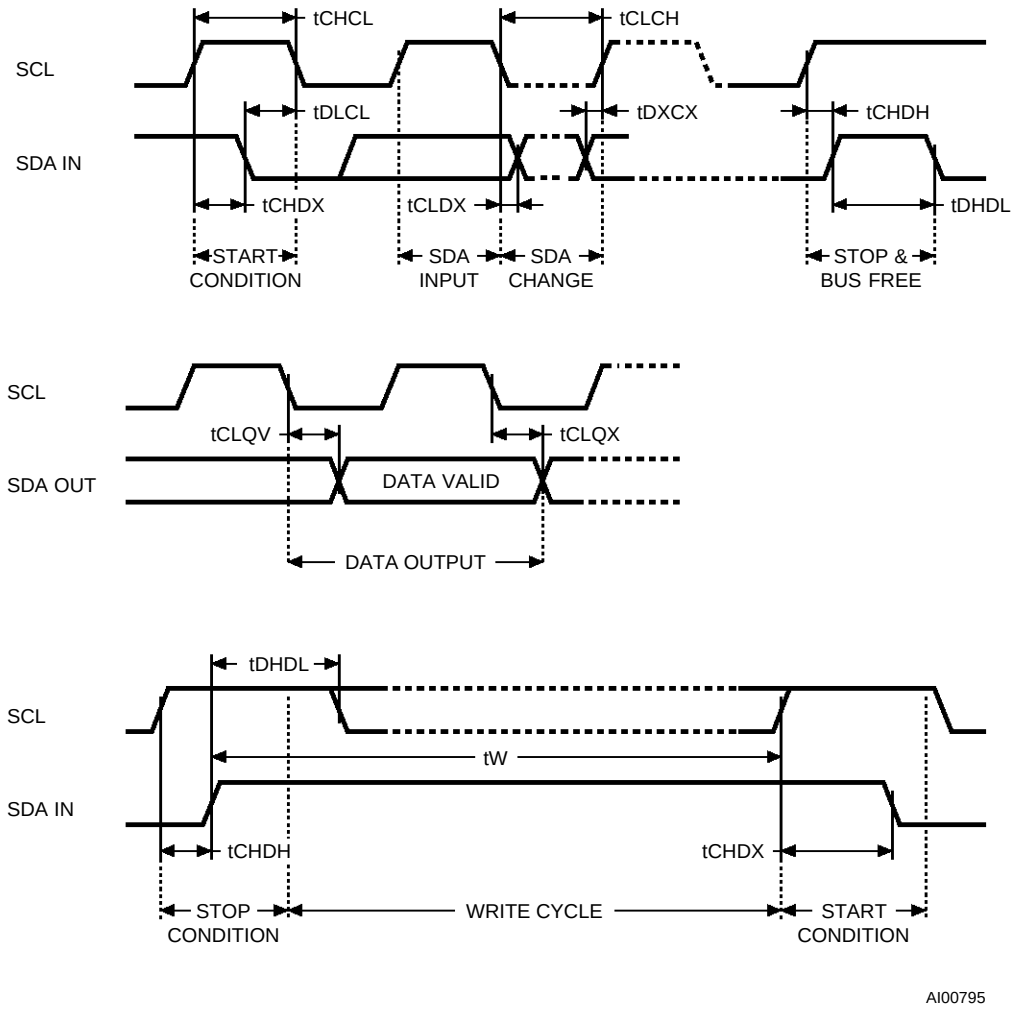


Memory Addressing. To start communication between the bus master and the slave M2201, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the 7th bit byte-address and a READ or WRITE bit. This 8th bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

Following a START condition the master sends the byte address with the $R\overline{W}$ bit reset to '0'. The memory acknowledges this and waits for a data byte. Any write command with $\overline{WC}$ = 1 (during a period of time from the START condition until the end of the Byte Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 8.

Figure 5. AC Waveforms



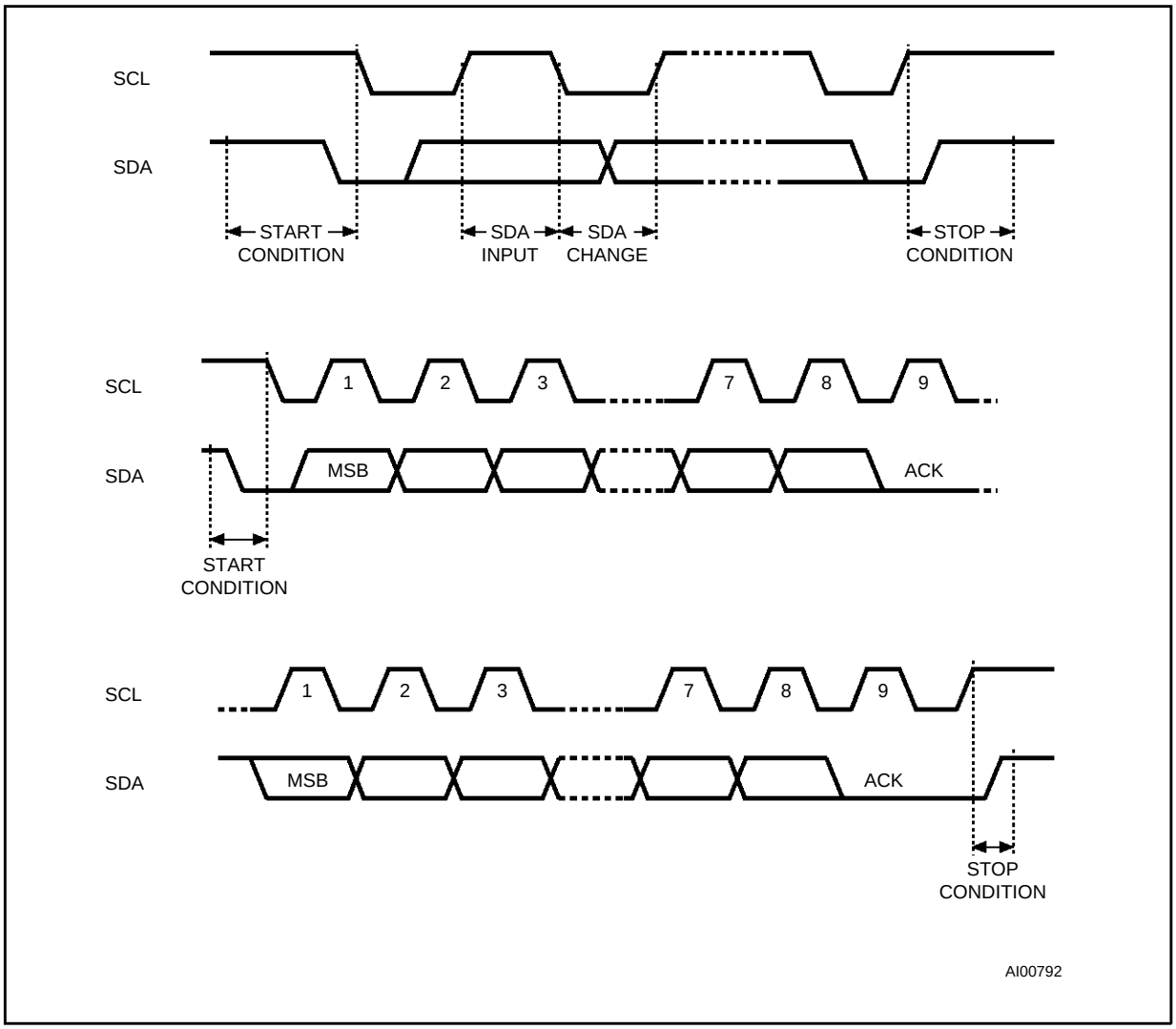
Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 4 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A6-A2) are the same. The master sends from one up to four bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (2 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

It must be noticed that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be re-

Figure 6. I^2C Bus Protocol

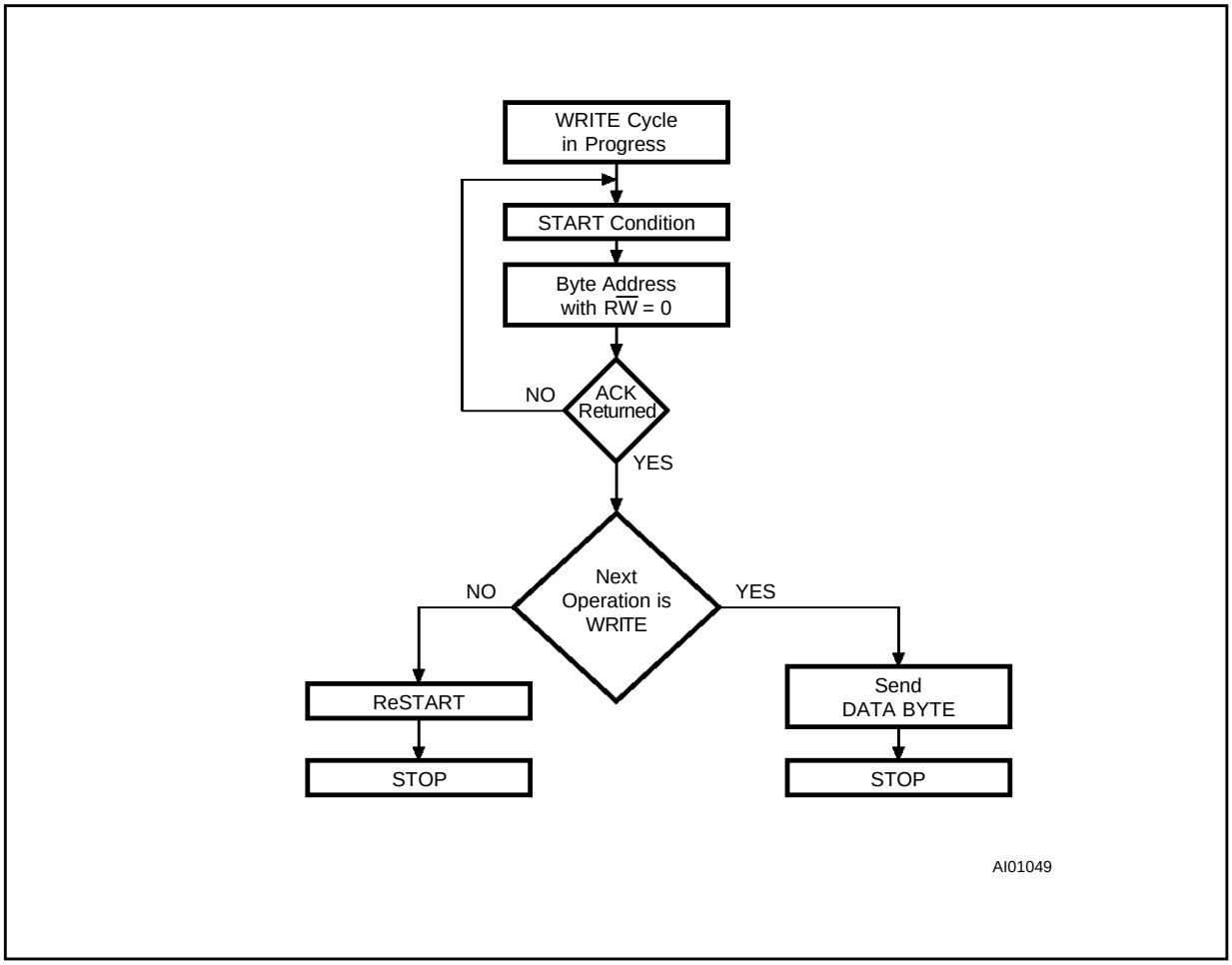


DEVICE OPERATION (cont'd)

duced by an ACK polling sequence issued by the master. The sequence is as follows:

– Initial condition: a Write is in progress (see Figure 7).
– Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
– Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Figure 7. Write Cycle Polling using ACK



Read Operation

Byte Read. The master sends a START condition followed by seven bits of address and the R/W bit (set to '1'). The M2201 acknowledges it and outputs the corresponding data byte. The read operation is terminated by a STOP condition issued by the master (instead of the ACK bit).

Sequential Read. The master sends a START condition followed by seven bits of address and the R/W bit (set to '1'). The M2201 acknowledges it and outputs the corresponding data byte. The master does acknowledge this byte and reads the next data byte (at address + 1). The read operation is terminated by a STOP condition issued by the master (instead of the ACK bit). The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over to address '00' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the M2201 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the M2201 terminates the data transfer and switches to a standby state.

Figure 8. Write Modes Sequences with Write Control = 1

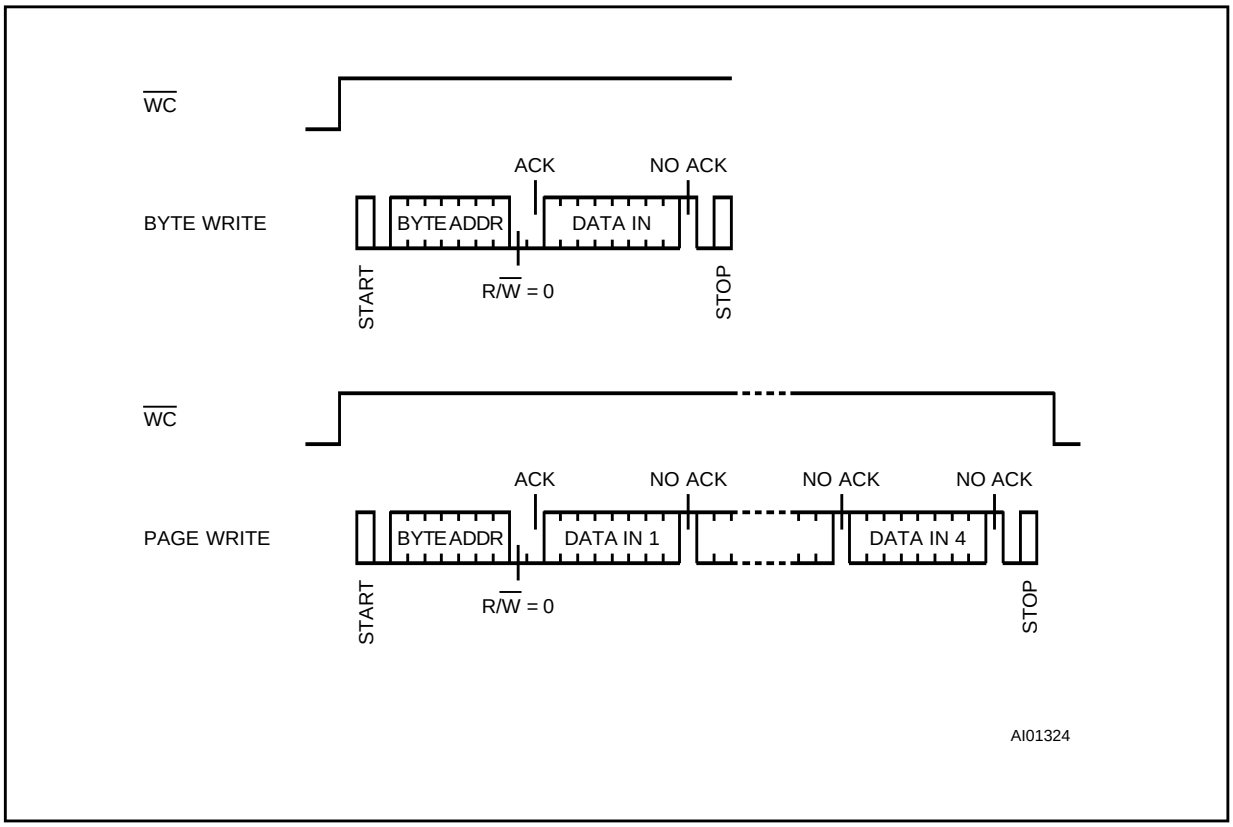
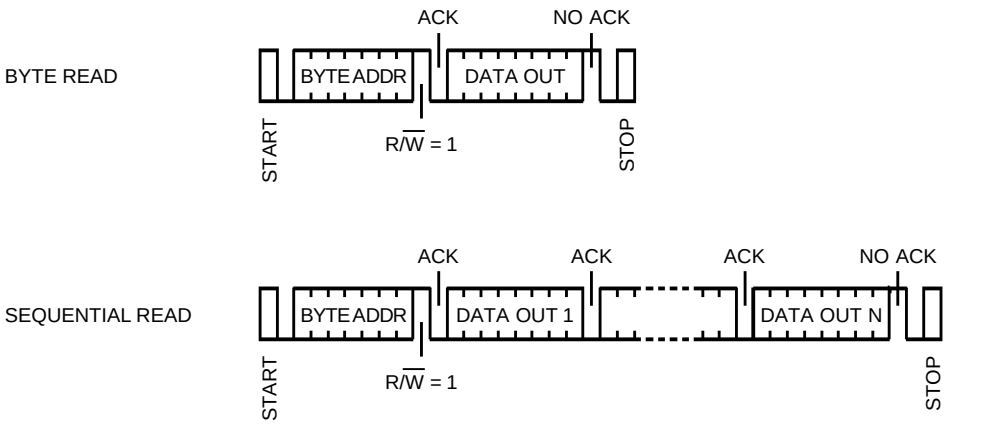


Figure 9. Read Modes Sequences



ORDERING INFORMATION SCHEME

Example: M2201 W M 1 TR

Operating Voltage		Package		Temperature Range		Option	
blank	4.5V to 5.5V	B	PSDIP8 0.25mm Frame	1	0 to 70 °C	TR	Tape & Reel Packing
W	2.7V to 5.5V	M	SO8	6	–40 to 85 °C		

Parts are shipped with the memory content set at all "1's" (FFh).

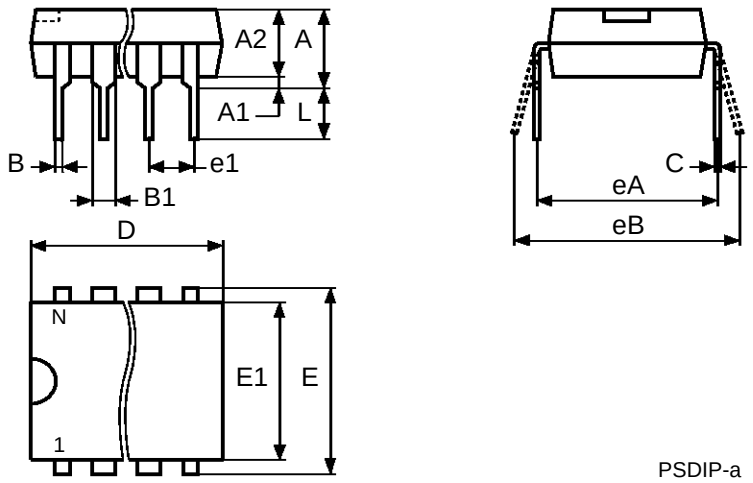
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



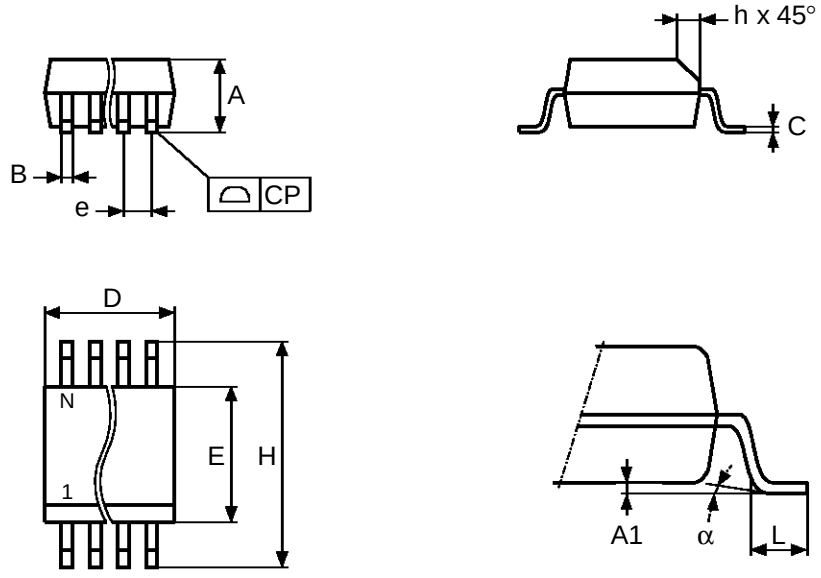
PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



SO-a

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